WHAT IS CLAIMED IS:

1.   A method for generating trace information of an
information processing device, wherein the information
processing device includes a processing unit and an
interface device, wherein the processing unit generates
operational information when branching occurs during
processing, and wherein the interface device has a buffer
circuit for receiving the operational information of the
branching from the processing unit, the method comprising
the steps of:

generating an absolute branching destination address
each time a branching occurs when the processing unit
performs processing;

storing the absolute branching destination address in
the buffer circuit;

generating a flag based on the absolute branching
destination address;

storing the flag in the buffer circuit in association
with the absolute branching destination address;

generating a relative branching destination address
based on the stored absolute branching destination address;
and

outputting, based on the flag, either one of the
absolute branching destination address and the relative
branching destination address.

2.   The method according to claim 1, further
comprising the steps of:

deleting a predetermined absolute branching destination
address stored in the buffer circuit when the absolute
branching destination addresses fully occupy the buffer
circuit; and

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shifting the flag associated with the deleted predetermined absolute branching destination address to output the absolute branching destination address.

5   3.   The method according to claim 2, further comprising the steps of:

based on the flag, serial-converting either one of the absolute branching destination address and the relative branching destination address; and

10   outputting the serial-converted branching destination address.

4.   An information processing device comprising:

a processing unit for generating a branching occurrence
15 signal and an absolute branching destination address each time a branching occurs during processing;

a determination circuit connected to the processing unit for comparing a formerly generated absolute branching destination address and a subsequently generated absolute
20 branching destination address and generating a flag in accordance with comparison result;

a buffer circuit connected to the processing unit and the determination circuit for sequentially associating the absolute branching destination address with the flag,
25 sequentially storing the associated absolute branching destination address and the flag, and outputting the absolute branching destination address and the flag in order stored; and

an output circuit connected to the buffer circuit for
30 generating a relative branching destination address based on the stored absolute branching destination address, wherein the output circuit outputs, based on the flag, either one of the absolute branching destination address and the relative

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branching destination address.

5.   The device according to claim 4, further
comprising:

5   a control circuit connected to the processing unit, the
determination circuit, and the buffer circuit for deleting a
predetermined absolute branching destination address stored
in the buffer circuit when the absolute branching
destination addresses fully occupy the buffer circuit and
10   for shifting the flag associated with the deleted
predetermined absolute branching destination address to
output the absolute branching destination address from the
output circuit.

15   6.   The device according to claim 5, wherein the
control circuit generates relative branching occurrence
state information or absolute branching occurrence state
information based on the branching occurrence signal and the
flag and generates address deletion state information when
20   an address in the buffer circuit is deleted.

7.   The device according to claim 4, wherein the
determination circuit computes a relative value between the
formerly generated absolute branching destination address
25   which is most recently stored in the buffer circuit and the
subsequently generated absolute branching destination
address received from the processing unit, and wherein
the determination circuit generates a first flag to
output the absolute branching destination address from the
30   output circuit when the relative value is included in a
predetermined range, and generates a second flag to output
the relative branching destination address from the output
circuit when the relative value is not included in the

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predetermined range.

8.   The device according to claim 4, wherein the
output circuit includes:

5   an absolute address buffer connected to the buffer
circuit for storing a first absolute branching destination
address received from the buffer circuit;

       a subtraction circuit connected to the absolute address
buffer and the buffer circuit for computing a relative
10   branching destination address using the first absolute
branching destination address and a second absolute
branching destination address, which is next output from the
buffer circuit after the first absolute branching
destination address;

15   a relative address buffer connected to the subtraction
circuit for storing the relative branching destination
address; and

       a serial-conversion circuit connected to the absolute
address buffer and the relative address buffer for serial-
20   converting either one of the first absolute branching
destination address and the relative branching destination
address and for thereafter outputting the serial-converted
branching destination address.

25   9.   An information processing device comprising:
       a processing unit for generating a branching occurrence
signal, an absolute branching destination address, and a
command fetch number each time a branching occurs during
processing;

30   a determination circuit connected to the processing
unit for comparing a formerly generated absolute branching
destination address and a subsequently generated absolute
branching destination address and generating a flag in

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accordance with comparison result;

a buffer circuit connected to the processing unit and the determination circuit for associating the absolute branching destination address with the flag and the command

5   fetch number, sequentially storing the associated absolute branching destination address, the flag, and the command fetch number, and outputting the absolute branching destination address, the flag, and the command fetch number in order stored; and

10   an output circuit connected to the buffer circuit for generating a relative branching destination address based on the stored absolute branching destination address, wherein the output circuit outputs the command fetch number and, based on the flag, either one of the absolute branching

15   destination address and the relative branching destination address.

10.   The device according to claim 9, further comprising:

20   a control circuit connected to the processing unit, the determination circuit, and the buffer circuit for deleting a predetermined absolute branching destination address stored in the buffer circuit when the absolute branching destination addresses fully occupy the buffer circuit and

25   for shifting the flag associated with the deleted predetermined absolute branching destination address to output the absolute branching destination address from the output circuit.

30   11.   The device according to claim 10, wherein the control circuit generates relative branching occurrence state information or absolute branching occurrence state information based on the branching occurrence signal and the

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flag and generates address deletion state information when an address in the buffer circuit is deleted.

12. The device according to claim 9, wherein the determination circuit computes a relative value between the formerly generated absolute branching destination address which is most recently stored in the buffer circuit and the subsequently generated absolute branching destination address received from the processing unit, and wherein the determination circuit generates a first flag to output the absolute branching destination address from the output circuit when the relative value is included in a predetermined range, and generates a second flag to output the relative branching destination address from the output circuit when the relative value is not included in the predetermined range.

13. The device according to claim 9, wherein the output circuit includes:
an absolute address buffer connected to the buffer circuit for storing a first absolute branching destination address received from the buffer circuit;
a subtraction circuit connected to the absolute address buffer and the buffer circuit for computing a relative branching destination address using the first absolute branching destination address and a second absolute branching destination address, which is next output from the buffer circuit after the first absolute branching destination address;
a relative address buffer connected to the subtraction circuit for storing the relative branching destination address; and
a serial-conversion circuit connected to the absolute

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address buffer and the relative address buffer for serial-
converting the command fetch number, outputting the serial-
converted command fetch number, serial-converting either one
of the first absolute branching destination address and the
5   relative branching destination address, and outputting the
serial-converted branching destination address.

        14.   An information processing system comprising:
        a processing unit for generating a branching occurrence
10   signal and an absolute branching destination address each
time a branching occurs during processing;
        a determination unit connected to the processing unit
for comparing a formerly generated absolute branching
destination address and a subsequently generated absolute
15   branching destination address and generating a flag in
accordance with the comparison result;
        a buffer unit connected to the processing unit and the
determination unit for associating the absolute branching
destination address with the flag, sequentially storing the
20   associated absolute branching destination address and flag,
and outputting the absolute branching destination address
and the flag in order stored; and
        an output unit connected to the buffer circuit for
generating a relative branching destination address based on
25   the stored absolute branching destination address, wherein
the output unit outputs, based on the flag, either one of
the absolute branching destination address and the relative
branching destination address.